Code No: **R41021**   **R10**   Set No. 1

IV B.Tech I Semester Supplementary Examinations, Mar/April - 2016
COMPUTER ORGANIZATION
(Electrical and Electronics Engineering)

Time : 3 hours   Max. Marks: 75

Answer any FIVE Questions
All Questions carry equal marks
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1 a) Perform the Arithmetic Operations (+42) + (-13) and (- 42) - (-13) in Binary using signed-2's Complement representation for negative numbers.   [8]
   b) Describe briefly the Connections between Processor and the Memory with a neat Diagram.   [7]

2 a) Represent the following conditional control statement by two register transfer statements with control functions.
       If (P=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3)   [8]
   b) Explain briefly about the Instruction Format of a Basic Computer.   [7]

3 a) A computer has 32-bit instructions and 12- bits addresses.
       If there are 250 two-address instructions, how many one-address instructions can be formulated?   [8]
   b) Explain Effective Address. List the Micro Operations performed by
         (i) AND to AC   (ii) ADD to AC   [7]

4 a) What are the design goals for a designer while deciding a Hardwired or Micro programmed Control unit for a CPU?   [8]
   b) With a block Diagram explain briefly the configuration of a Micro programmed control unit.   [7]

5 a) Give a block Diagram for organization of a 2M X 32 Memory module using 512k X 8 Static Memory chips.   [8]
   b) Write short note on Associative- mapped Cache.   [7]

6 a) With a neat Diagram explain the communication link between the Processor and several Peripherals.   [8]
   b) Explain the concept of Handshaking technique.   [7]

7 a) Draw a space-time Diagram for a six-segment pipeline showing the time it takes to process eight tasks.   [8]
   b) Differentiate between Arithmetic Pipeline and Instruction Pipeline.   [7]

8 a)   Discuss the difference between tightly coupled Multiprocessors and loosely coupled Multiprocessors from the viewpoint of hardware organization and programming techniques.   [8]
   b) Write short note on Hypercube Interconnection.   [7]